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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,894	07/28/2003	Yi-Nan Chen	10112581	7425
34283	7590	12/23/2004	EXAMINER	
QUINTERO LAW OFFICE 1617 BROADWAY, 3RD FLOOR SANTA MONICA, CA 90404			PHAM, THANH V	
			ART UNIT	PAPER NUMBER
			2823	

DATE MAILED: 12/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/628,894

Applicant(s)

CHEN ET AL.

Examiner

Thanh V Pham

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pm

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 November 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
2. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Forster et al. US 6,455,369 B1 in combination with Wolf et al., Silicon Processing for the VLSI Era, Vol. 1.

Re claims 1, 5 and 8- 9 and 15 and 18, the Forster et al. reference discloses a first method for fabricating a trench capacitor comprising:

forming a trench in a substrate, fig. 1A;

filling a lower portion of the trench with a conductive S5 layer surrounded by a doped layer S4, fig. 1D;

forming a conformable silicon nitride S6 layer overlying the substrate and an inner surface of an upper portion of the trench to cover the conductive layer and the doped layer, fig. 1F;

performing a heat treatment on the substrate to form a doping region S7 therein and around the doped layer, fig. 1G;

anisotropically etching the silicon nitride layer to form a collar silicon nitride layer over the sidewall of the upper portion of the trench, col. 10, ll. 2-3;

successively removing the conductive layer and the doped layer using the collar silicon nitride layer using the collar silicon nitride layer as a mask to expose the surface of the doping region, fig. 1H;

forming a conformable rugged polysilicon layer S8 in the lower portion of the bottle-shaped trench, fig. 1I; and

filling the lower portion of the bottle-shaped trench with a first doped-polysilicon layer S11 to serve as a top plate, fig. 1N.

The first method of Forster et al. lacks the steps of partially oxidizing the exposed doping region to form a doped oxide region thereon and removing the doped oxide region to form a bottle-shaped trench. However, the third through fifth methods disclose, after removing the conductive S5, "the lower trench region is widened by means of a further etching step in order to enlarge the electrode surface, as is illustrate in FIG. 5I", col. 13, lines 55-58, e.g.

One of ordinary skill in the art would seek a way to further etching the lower trench region to enlarge the electrode surface as suggested by Forster et al.'s fifth method; and Wolf et al. provides a wet etching silicon dioxide with various hydrofluoric acid (*re claims 5 and 15*) (page 532) after recognizes the thermal processing includes rapid thermal processing (pages 56-58) (*re claims 8 and 18*), "the density of thermally grown fused silica is less than that of crystalline quartz" (page 200) and "diffusion in an oxidizing ambient can result in oxidation enhanced diffusion or oxidation retarded diffusion" (page 264).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ an oxidizing and etching steps of Wolf et al. in the combination of the first and fifth method of Foster et al. as the oxidizing and etch steps would be selected in accordance with the trench capacitor formation in order to enlarge the electrode surface as taught by Foster et al.

Re claims 2 and 20, the Forster et al. reference discloses further performing a gas phase doping after the rugged polysilicon layer is formed, col. 10, lines 17-20.

Re claim 3, the Forster et al. reference discloses the conductive layer is a polysilicon layer, col. 9, line 56.

Re claims 4 and 14, the Forster et al. reference discloses the doped layer is an arsenic silicate glass layer, col. 9, line 54.

Re claims 6 and 16, the combination does not disclose the silicon nitride layer has a thickness of about 300-400 angstroms. Choice of about 300-400 angstroms for the silicon nitride to achieve particular device properties would have been a matter of routine optimization because a layer thickness are known to affect device properties and would depend on the desired device density on the finished wafer and the desired device characteristics. One of ordinary skill in the art would have been led to the recited thickness through routine experimentation to achieve the desired device density (MPEP 2144.05).

Re claims 7 and 17, the Forster et al. reference discloses "by means of baking, arsenic is then outdiffused from the arsenic glass layer S4 into the silicon substrate S1" (col. 9, lines 65-66) but not disclose the heat treatment is performed at about 900-1100

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°C, the Wolf et al. reference discloses "dopants were diffused to the desired depths by subjecting to elevated temperatures (900-1200 °C)" (page 242). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the elevated temperature of Wolf et al. in the baking of Forster et al. as the temperature would be selected in accordance with the trench capacitor formation in order to have a buried plate as taught by Foster et al.

Re claim 10, the Forster et al. reference further discloses removing the collar silicon nitride layer S6, fig. 1N; forming a collar silicon oxide layer S12 over the upper portion of the sidewall of the bottle-shaped trench; and successively filling the upper portion of the bottle-shaped trench with a second doped polysilicon layer and a third doped polysilicon layer, fig. 1O and col. 10, ll. 35-62.

Re claim 11, the Forster et al. reference discloses the masking layer is composed of a pad oxide layer S2 and an overlying silicon nitride layer S3, fig. 1A.

Re claim 19, the Forster et al. reference discloses the capacitor dielectric layer comprises a silicon nitride layer S10, fig. 1L.

Re claim 12, the combination does not disclose forming a recess at the pad oxide layer and filling the recess with silicon nitride. The Ho et al. reference discloses before filling the trench further comprising the steps of: etching the pad oxide layer 20 to form a recess, fig. 1e; and filling the recess with silicon nitride 50 before further steps to form a trench capacitor, figs. 1g-1m.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply a further step of Ho et al. in the combination process as the nitride

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filling step at the pad oxide would be selected in order to enforce the nitride from peeling in accordance with the process of forming trench capacitor as taught by the combination.

Response to Arguments

3. Applicant's arguments filed 11/04/04 have been fully considered but they are not persuasive.

4. The applicant states: "The references cannot be combined in the manner relied upon by the office action because the prior art does not teach the desirability of the combination". The examiner does not agree. And in response to the argument on page 2, the following is provided.

Firstly, Forster et al. desire "the lower trench region is widened by means of a further etching step" as recognized by the applicant in the Request for Reconsideration, page 1, next-to-last paragraph.

Secondly, Wolf et al. have recognized the thermal processing including rapid thermal processing wherein "the density of thermally grown fused silica is less than that of crystalline quartz" and "diffusion in an oxidizing ambient can result in oxidation enhanced diffusion or oxidation retarded diffusion", provides a wet etching silicon dioxide with varied hydrofluoric acid. Applicant recognizes half of these facts in the bridged paragraph of page 1 and page 2 by ignoring the provided sequential facts in the previous Office action mailed 08/12/04. One of ordinary skill in the art would seek a way to further etching the lower trench region to enlarge the electrode surface as suggested

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by Forster et al.'s fifth method *without or least affected to the surrounding substrate*; and Wolf et al. provides a surface preparation so that "silicon oxide may have a more open structure than the crystalline silicon oxide due to the lower density and may be removed by HF acid" (acknowledged by the applicant in the bridged paragraph of page 1 and page 2). The HF etch would be made easier and controllable in this aspect.

5. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). In this instant, motivation is a statement of Forster et al., "the lower trench region is widened by means of a further etching step in order to enlarge the electrode surface, as is illustrate in FIG. 5I", col. 13, lines 55-58, e.g.; and Wolf et al. after recognizes the thermal processing includes rapid thermal processing (pages 56-58), "the density of thermally grown fused silica is less than that of crystalline quartz" (page 200) and "diffusion in an oxidizing ambient can result in oxidation enhanced diffusion or oxidation retarded diffusion" (page 264), Wolf et al. provides a wet etching silicon dioxide with varied hydrofluoric acid (page 532).

6. In response to applicant's arguments against the references individually (page 4), one cannot show nonobviousness by attacking references individually where the

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rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

7. In response to applicant's argument that "neither Forster et al. nor Wolf et al., whether taken alone or in combination, teach or suggest partially oxidizing an exposed doping region to form a doped oxide region thereon, and removing the doped oxide region to form a bottle-shaped trench", the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

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shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh V. Pham whose telephone number is 571-272-1866. The examiner can normally be reached on M-Th (6:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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George Fourson
Primary Examiner